13. (CANCELED)

21. (TWICE AMENDED) A system for carrying out simulation of a circuit, comprising:

a data input unit inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

a circuit extracting unit extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

a storage unit holding data concerning configurations of the plurality of partial circuits; and

a circuit equivalence inspecting unit detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits on the basis of the configurations of the plurality of partial circuits, and having a judging unit judging equivalence when the configurations of said plurality of partial circuits are mutually consistent,

wherein the circuit to be simulated is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and circuit simulation is performed on the compressed circuit.

25. (CANCELED)

33. (TWICE AMENDED) An apparatus for carrying out simulation of a circuit, comprising:

a data input circuit inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

a circuit extracting circuit extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

a storage circuit holding data concerning configurations of the plurality of partial circuits; and

a circuit-equivalent inspecting circuit detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits on the basis of the configurations of the plurality of partial circuits, and having a judging circuit judging equivalence when the configurations of said plurality of partial circuits are mutually consistent,

wherein the circuit to be simulated is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and circuit simulation is performed on the compressed circuit.

37. (CANCELED)

45. (CANCELED)

REMARKS

Claims 9-45 are pending in this application and have been rejected. Claims 9, 21, and 33 have been amended. Claims 13, 25, 37 have been cancelled and included in claims 9, 21, and 33, respectively. Claim 45 has also been cancelled. No new matter is being presented, and approval and entry are respectfully requested.

Rejections Under §§ 101 and 112

On June 7, 2001, the undersigned conducted an Examiner Interview with Examiner Jones. The Examiner was very helpful. During the Examiner Interview, the Examiner agreed to withdraw the §101 rejection and all §112 rejections issued in the final Office Action mailed January 16, 2001, except those §112 rejections directed to "compressing" and "integrating." The Examiner requested additional explanation of these terms and their locations within the present specification.

Accordingly, the present invention compresses or reduces a circuit to be simulated by integrating or combining partial circuits that have equivalent operational characteristics (i.e., the same types of circuit components, component characteristics, and connectional relationships of the input and output terminals) into one circuit. The purpose of compressing a circuit is to simplify the circuit that is simulated, thereby reducing the time required for simulation. This type of circuit compression has been described in Japanese Patent Application No. 8-198074 filed July 26, 1996 by the same inventor, as noted on page 2 of the present specification.

One example of circuit compression can be found in Fig. 2 and the accompanying text on pages 2-4 of the specification. In Fig. 2(A), two partial circuits, each containing an NMOS transistor, have been determined to have equivalent operational characteristics. Thus, the two partial circuits are integrated into one partial circuit, as shown in Fig. 2(B). Another example of